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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,366	01/14/2004	Hiroaki Nakano	TAI 146	2358

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,366	NAKANO, HIROAKI	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6 and 23-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 23-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 23 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheah (6,894,229).

Regarding claim 1, Cheah teaches in figure 1A and related text a circuit board comprising:

a semiconductor chip 110;

at least one wiring 124 electrically connected to said semiconductor chip;

at least one reinforcement layer 140 for maintaining a strength of the circuit board :

an insulating substrate 120 having a surface that is defined by mutually non-overlapping regions, the regions including

a semiconductor chip region, the semiconductor chip being mounted over the semiconductor chip region,

at least one wiring region, the wiring being formed on said at least one wiring region, with at least a portion of the wiring being not covered by the semiconductor chip, and

at least one reinforcement layer region, the reinforcement layer being formed on said at least one reinforcement layer region; and

a protective film 144 that covers the wirings and the reinforcement layer.

Regarding claim 23, Cheah teaches in figure 1A and related text a circuit board for mounting a semiconductor chip, wherein none of the wiring is covered by the semiconductor chip.

Regarding claim 25, Cheah teaches in figure 1A and related text a semiconductor chip, wherein the semiconductor chip has a terminal on an upper surface thereof; further comprising a bonding wire 130 that extends from the terminal to the wiring to electrically connect the semiconductor chip to the wiring.

Claims 6, 27-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Pu et al. (6,828,665).

Pu et al. teach in figure 2 and related text a method of manufacturing a circuit board comprising:

Providing an insulating substrate 51 having a surface, the surface including mutually non-overlapping regions, the regions including a semiconductor chip region, at least one reinforcement layer region and at least one wiring region:

forming a wiring 51c in the wiring region and adjacent to the semiconductor chip region;

forming a reinforcement layer 55 (metal pin 55 is a reinforcement layer because it supports the structure) in the reinforcement layer region and adjacent to the wiring region;

forming a protective film 56 that covers the wirings and the reinforcement layer, and which covers the semiconductor chip region;

after the protective film is formed, mounting a semiconductor chip 500 on the protective film and over the semiconductor chip region; and

electrically connecting the wiring to the semiconductor chip, wherein

the mounting of the semiconductor chip includes positioning the semiconductor chip so that at least a portion of the wiring is not covered by the semiconductor chip, wherein

none of the wiring is covered by the semiconductor chip, and wherein

an upper surface of the protective film is not planar over the wiring and the reinforcement layer, and is planar under the semiconductor chip.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 24, 26 and 31-36, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibamoto et al. (2002/0105070) in view of Baba (6,046,077). Regarding claims 1 and 31, Shibamoto et al. teach in figure 15 and related text a circuit board comprising:

a semiconductor chip 1;

at least one wiring 10 electrically connected to said semiconductor chip;

at least one reinforcement layer 3 for maintaining a strength of the circuit board :

a substrate (see paragraph [36]) having a surface that is defined by mutually non-overlapping regions, the regions including

a semiconductor chip region, the semiconductor chip being mounted over the semiconductor chip region,

at least one wiring region, the wiring being formed on said at least one wiring region, with at least a portion of the wiring being not covered by the semiconductor chip, and

at least one reinforcement layer region, the reinforcement layer being formed on said at least one reinforcement layer region; and

a protective film 8 that covers the wirings and the reinforcement layer.

Shibamoto et al. do not state that the substrate is an insulating substrate.

Baba teaches in figure 15 and related text an insulating substrate 4.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an insulating substrate in Shibamoto et al.'s device I order to use the device in its intended use, by using conventional substrate.

Regarding claims 24 and 26, Shibamoto et al. teach in figure 15 and related text a protective film disposed under the semiconductor chip and supports the semiconductor chip over the semiconductor chip region, with the semiconductor chip being separated from the wiring and from the surface of the insulating substrate by the protective film,

wherein the protective film is disposed under the semiconductor chip, and wherein an upper surface of the protective film is not planar over the wiring and the reinforcement layer, and is planar under the semiconductor chip.

Regarding claim 31, Shibamoto et al. teach in figure 15 and related text a protective film that covers the substrate, the wiring and the reinforcement layer to protect them; a semiconductor chip arranged over the chip mounting region and on the protective film; a bonding wire that connects the semiconductor chip to the wiring; and a sealing resin that seals at least the bonding wire and the semiconductor chip.

Regarding claims 32-36, prior art's device comprises: a protective film has a shape corresponding to the surfaces of the wiring, the reinforcement layer and the substrate,

solder balls provided on a rear surface of the substrate, wherein

the solder balls are electrically connected with the wiring, wherein

the wiring comprises copper, wherein

the solder balls are provided at positions on the rear surface of the substrate corresponding to the wiring region, wherein

the protective film is a solder resist, wherein

a surface of a portion of the protective film positioned in the chip mounting region is planar.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. Pu et al. teach substantially the entire claimed structure, as applied to claim 6 above, except the electrically connecting the wiring to the semiconductor chip includes extending a bonding wire from a terminal on an upper surface of the semiconductor chip 500, to the wiring.

Pu et al. teach in figure 2 electrically connecting the wiring to the semiconductor chip includes extending a bonding wire 53 from a terminal on an upper surface of the semiconductor chip 52, to the wiring 51C.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to extend a bonding wire from a terminal on an upper surface of the semiconductor chip 500, to the wiring in Pu et al.'s device in order to use the device in an application which comprises chips with upper external connections.

Response to Arguments

Applicant's arguments with respect to claims 1, 6 and 23-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-F are cited as being related to packaging devices having stiffeners.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
6/8/06

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PRIMARY EXAMINER
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